CLAIM OR CLAIMS

WHAT IS CLAIMED IS:

1. A dither system for a quantizing device comprising:

means for obtaining a dither signal from a clock signal having a sample frequency, the dither signal having a frequency that is one-third of the sample frequency;

means for combining the dither signal with an analog signal to be digitized at an input to the quantizing device;

means for generating from a digital version of the dither signal from the obtaining means a cancellation signal; and

means for combining the cancellation signal with a digital output signal from the quantizing device to produce a corrected digital output signal having reduced quantization distortion.

2. The dither system as recited in claim 1 wherein the obtaining means comprises:

a divide-by-three circuit having the clock signal as an input and the digital version of the dither signal as an output; and

means for filtering the digital version of the dither signal to produce as an output the dither signal for input to the dither signal combining means.

3. The dither system as recited in claim 2 wherein the obtaining means further comprises a low-jitter clock re-timing register having as an input the

digital version of the dither signal and having as an output a re-timed digital version of the dither signal for input to the filtering means.

4. The dither system as recited in any of claims 1-3 wherein the cancellation signal generating means comprises:

means for translating the digital version of the dither signal into a direct digital version;

means for delaying the direct digital version by one cycle of the clock to produce a quadrature digital version;

means for multiplying the direct and quadrature digital versions by respective programmable coefficients to produce quadrature digital products; and

means for combining the quadrature digital products to produce the cancellation signal.